IN THE CLAIMS

1. (currently amended): An intermediary of a semiconductor device, comprising:

a semiconductor substrate having a surface formed with a first trench; ~~recessed region;~~

a first dielectric material formed in the first ~~recessed region~~ trench, wherein the first dielectric material substantially fills the first trench;

~~a second recessed region formed within the first dielectric material, wherein the second recessed region has walls, a lower surface, and a first opening in proximity to the surface; and~~

a polycrystalline semiconductor layer formed overlying the first dielectric material and having a ~~second~~ first opening; and

a second trench etched into the first dielectric material through the first opening, wherein the second trench has walls, a lower surface and a second opening, and wherein the first opening at least partially overlies ~~overlying~~ the ~~first~~ second opening, and wherein the polycrystalline semiconductor layer and the second trench ~~recessed region~~ are configured to form a region of reduced substrate capacitance.

Claims 2-4 (cancelled).

5. (previously presented): The intermediary of claim 1, wherein the polycrystalline semiconductor layer comprises polysilicon.

6. (previously presented): The intermediary of claim 1, wherein the first dielectric material includes deposited silicon dioxide.

7. (currently amended): The intermediary of claim 1, further comprising a layer of material formed ~~overlying~~ lining the walls of the second trench. ~~recessed region.~~

8. (previously presented): The intermediary of claim 1, wherein the first dielectric material is recessed below a major surface of the semiconductor substrate.

9. (previously presented): The intermediary of claim 8, wherein the first dielectric material is recessed below the major surface a distance of about 0.5 microns.

10. (previously presented): The intermediary of claim 7, wherein the layer of material comprises polycrystalline silicon.

Claims 11-25 (cancelled).

26. (currently amended): An intermediary of a semiconductor device, comprising:

a semiconductor substrate having a surface formed with a first trench; ~~recessed region;~~

a first dielectric material deposited in the first trench, wherein the first dielectric material substantially fills the first trench; ~~recessed region and formed with a second recessed region having a first opening and walls; and~~

a polysilicon cap layer formed overlying the first dielectric material and having a first ~~second~~ opening; and

a second trench etched into the first dielectric material through the first opening, wherein the second trench has a second opening adjacent the first opening, and ~~at least partially overlying the first opening,~~ wherein the polysilicon cap layer and the second trench ~~recessed region~~ are configured to form a region of reduced substrate capacitance.

Claims 27-28 (cancelled).

29. (currently amended): The intermediary of claim 26, wherein the ~~first~~ second opening is wider than the first ~~second~~ opening.

Claims 30-31 (cancelled).

32. (currently amended): The intermediary of claim 26, wherein the second trench ~~recessed region~~ is formed having a layer of material deposited on ~~the~~ walls of the second trench.

33. (previously presented): The intermediary of claim 32, wherein the layer of material includes polycrystalline silicon.